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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,722	04/13/2004	Kenji Yoneda	60188-834	2871

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EXAMINER	
EVERHART, CARIDAD	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,722	YONEDA, KENJI	
	Examiner	Art Unit	
	Caridad M. Everhart	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4-13-2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Huber(US 4,868,133)

Huber discloses the steps of performing a first thermal treatment on a wafer at a temperature of 600-750 degrees C(col. 6,lines 18-24) for a time of 15-360 minutes(col. 6,lines 25-27), which includes the recited range. This step is carried out first(col. 6,lines

53-57). Then there is the step of performing a second thermal treatment at 900-1300 degrees C(col. 5, lines 20-22). It can be seen in Table 2, col. 8, that the high temperature thermal treatment may be for 30 minutes, as there is a line in the table of 900 degrees C for thirty minutes. The wafers are silicon (col. 3,lines 58-59) and the disclosure that these are untreated wafers(col. 5,line 5) indicate that this is the first step in the fabricating process. The cooling rate of the wafer is within the recited range(col. 6,lines 10-15). The heating rate for the first step is within the recited range(col. 6,lines 34-38).

Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Aoki(us 4,944,399).

Aoki discloses that in the gettering of metals from a semiconductor substrate there is a defect layer, which satisfies the limitation of a BMD, because the layer is a layer of bulk microdefects as is understood in the art, formed for gettering and there is a defect-free zone(col. 1, ines 53-57). Aoki discloses that the depth(called width, which is used for depth) of the denuded zone is given the same dimension as the diffusion distance of the metal which it is desired to getter, in this case Fe(col. 5,lines 40-50) and in this cited portion of Aoki it is disclosed that the depth of the zone is calculated to be the diffusion length of the Fe.

Claim Rejections - 35 USC § 103

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huber as applied to claim 1 above and further in view of Satoh, et al. (US 5,674,756).

Huber is silent with respect to the recited ramping rate for the second heating step, although Huber does teach the recited heating rate for the first heating step and the recited cooling rate.

Satoh, et al discloses heat treatment of a silicon wafer in the recited temperature ranges with ramping up of 2-10 degrees C which includes the recited range(col. 2, lines 55-60) and for time that includes the recited range(col. 2,lines 58-60). The time held at the first temperatue is also within the recited range (col. 2,lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the ramping rate recited by Satoh, et al in the method taught by Huber because the ramping rate is a variable of the art which one of ordinary skill in the art would be able to determine and because it is recommended by Satoh, et al in order to achieve improved results(col. 2, lines 57-64).

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huber as applied to claim 1 above, and further in view of Gardner, et al. (US 5,795,809).

Huber is silent with respect to the recited further steps.

Gardner et al discloses that in a CMOS process there are steps that are high-temperature steps in which the metal impurities are diffused to the gettering sites(col. 9, lines 52-57). In addition, a CMOS process would include the formation of gate oxide layer, as there are gates formed in a CMOS process(col. 1,lines 35-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the steps taught by Gardner et al with the steps in the

process taught by Huber because the formation of CMOS devices is one of the uses of silicon wafers which is conventional in the art, and the steps taught by Gardner et al are steps in the formation of CMOS devices on a silicon substrate with oxygen gettering nucleation sites.

Claims 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huber in view of Gardner, et al as applied to claims 3 and 6 above, and further in view of Falster, et al. (US 5,403,406).

Huber in view of Gardner, et al is silent with respect to the recited depth of the oxygen nucleation site layer nor the recited concentrations . Huber in view of Gardner, et al does disclose in Gardner, et al that the thermal budget is preserved for the characteristics of the semiconductor device, in that in Gardner et al the thermal steps for other processes of forming the semiconductor device are combined with the thermal steps for the oxygen gettering sites, so that additional thermal steps need not be performed(Fig. 12, steps 104, 106, and 108) .

Falster teaches that there is a band of oxygen sites in the substrate (Fig. 3), as Falster shows that there is at a certain depth a high concentration of the sites, and Falster teaches that the thermal treatment conditions control the depth of the band of sites(col. 5, lines 1-2). In addition, the Fig. Shows that one can obtain a concentration within the recited range.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method taught by Falster with the process taught by Huber in view of Gardner because this would be a method of optimizing the process in

order to achieve desired properties of the substrate, and optimization is a well known step in engineering processes.

With respect to the thermal treatments being set within a range that maintains the characteristics of the semiconductor device, this would also have been obvious to one of ordinary skill in the art, because otherwise there would be damage to the device, which would then be detrimental to the process, and the maintaining of the thermal budget was suggested by Gardner, et al, as cited above.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huber in view of Falster as applied to claim 4 above further in view of Aoki as applied to claim 8 above.

Huber in view of Falster does not teach the depth related to the diffusion distance.

Aoki discloses relation of the depth to diffusion distance, as relied upon above.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teaching of Aoki with respect to the depth of the BMD with the method and device taught by Huber in view of Falster in order to obtain optimization of the gettering as taught by Aoki by the use of the diffusion distance.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huber in view of Falster et al further in view of Aoki as applied to claim 4 above, and further in view of Miyashita, et al. (US 5,951,755).

Huber in view of Falster et al further in view of Aoki is silent with respect to an epitaxial layer on the substrate.

Miyashita, et al discloses a BMD layer under an epitaxial layer in the formation of a semiconductor device(Figures 2A and 2B and col. 10, lines 50-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the epitaxial layer at a depth which is smaller than the diffusion distance of the ions which are being gettered in the process taught by Huber in view of Falster et al further in view of Aoki because Miyashita teaches the formation of an epitaxial layer in the formation of a semiconductor device and because Aoki teaches gettering from a region adjacent to the surface of a silicon wafer(col. 2,lines 17-20), which would include an epitaxial layer , since the epitaxial layer is adjacent to the silicon surface, and the distance for the epitaxial layer would apply just as in the method taught by Aoki.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 571-272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, B. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CARIDAD EVERHART
PRIMARY EXAMINER

C. Everhart
4-22-2005